NAVY STTR
PROPOSAL SUBMISSION

INTRODUCTION:

The responsibility for the implementation, administration and management of the Navy STTR program is with the Office of Naval Research (ONR). The Navy STTR Program Manager is Mr. John Williams, (703) 696-0342. All STTR Phase I and Phase II proposals, Phase I and II printed electronic summary reports, as well as Phase III Success Stories should be forwarded to Mr. Williams at the address below. If you have any questions, problems following the submission directions, or inquiries of a general nature, contact Mr. Williams. All Phase I proposals are due by **12 April 2000** and must be submitted to:

Office of Naval Research
ATTN: Mr. John Williams, ONR 364 STTR
800 North Quincy Street
Arlington, VA 22217-5660

UNIQUE NAVY REQUIREMENTS:

1. The Navy requires a " DOD Proposal Cover Sheet" (formerly Appendix A & B) to be submitted electronically through the Navy SBIR/STTR Website or DOD SBIR/STTR Website at http://www.dodsbir.net/sbirsubmission. The company must print out the forms directly from the Website, sign the forms and submit them with their proposal.
2. All Phase I award winners must electronically submit Phase I Summary Report(s) through the Navy SBIR /STTR Website at the end of their Phase I.
3. The Navy requires that all invited Phase II proposers submit a Proposal Cover Sheet and Commercialization Report through the DoD SBIR Submission Website. Mail a printed and signed copy of the Proposal Cover Sheet and Commercialization Report only to the Navy STTR Program Office listed above. Mail the full Phase II proposal with Proposal Cover Sheet and Commercialization Report to the sponsoring Navy activity and technical point of contact.
4. Phase II award winners must also submit Phase II summary reports through the Navy SBIR/STTR Website.
5. The requirements and time frames for Navy Fast Track submission have been modified and are described below.
6. The Navy only accepts proposals with a base effort not exceeding $70,000 with an option not exceeding $30,000. Phase I base effort should run about 6 months and the option 3 months.

NEW THIS YEAR:

1. The Small Business Administration (SBA) has made a determination that will permit the Naval Academy, the Navy Post-Graduate School and other military academies to participate as the research institution or subcontractor in the SBIR/STTR program, since they are institutions of higher learning.

2. The Navy will allow firms to include with their proposals success stories that have been submitted through the Navy SBIR/STTR Website at (**http://www.onr.navy.mil/sbir**). A Navy Success Story is any follow-on funds that the firm has received from a past Phase II Navy SBIR or STTR award. To qualify, the firm must submit these success stories no later than **15 March 2000,** through the Navy SBIR/STTR Website. The success story should then be printed and included as an appendix to the proposal. These pages will not be counted towards the 25-page limit. The success story information will be used as part of the evaluation of the third criteria, Commercial Potential (listed in Section 4.2 of this solicitation) which includes the Company Commercialization Report (formerly Appendix E) and the strategy described to commercialize the technology discussed in the proposal. Commercialization is viewed as any follow-on funds, from the DOD, DOD contractors or the private sector, used to further develop the technology or from sales of a product. The Navy is very interested in companies that transition SBIR/STTR efforts directly into Navy and DOD programs and/or weapon systems. If a firm has never received a Navy SBIR/STTR Phase II award, it will not count against them and they will be evaluated on the other evaluation criteria listed in Section 4.2 Phase I Evaluation Criteria. If you have any questions about this requirement, call John Williams at (703) 696-0342.

YOUR SUBMISSION TO THE NAVY STTR PROGRAM:

This solicitation contains a mix of topics. When preparing your proposal keep in mind that Phase I should address the feasibility of the solution to the topic. Phase II is the demonstration of the technology that was found feasible in Phase I. Only those Phase I awardees which have been invited to submit a Phase II proposal by the Navy technical point of contact (TPOC) during or at the end of a successful Phase I effort will be eligible to participate for a Phase II award (with the exception of Fast Track Phase II proposals per section 4.5). If you have been invited to submit a Phase II proposal to the Navy by the TPOC, obtain a copy of the Phase II instructions from the Navy SBIR/STTR Bulletin Board on the Internet or request the instructions from the Navy STTR Program Office. All Phase I and Phase II proposals should be sent to the Navy STTR Program Office (at the above address) for proper processing. Phase III efforts should also be reported to the STTR program office noted above.

The Navy will provide potential awardees the opportunity to reduce the gap between Phases I and II if they provide a $70,000 maximum feasibility Phase I base proposal and a fully costed, well defined ($30,000 maximum) Phase I option to the Phase I. **The Navy will not accept Phase I proposals in excess of $70,000 (exclusive of the Phase I option).** The technical period of performance for the Phase I base effort should be 6 months and for the Phase I option should be 3 months. Plan for the 6 month awards to be made for the period of approximately June 1 through December 1. The Phase I option should be the initiation of the next phase of the STTR project (i.e. initial part of Phase II), and it must be included with the Phase I proposal. Please include brief task statements and milestones for the Phase I option, and include the costs on the same Cost Proposal, but in a separate column.

If you are invited to submit a Phase II proposal, it should consist of three elements: 1) a $400,000 maximum demonstration phase of the STTR project; 2) a transition or marketing plan (formally called a "commercialization plan") describing how, to whom and at what stage you will market your technology to the government and private sector; 3) a Phase II option ($100,000 maximum) which would be a fully costed and well defined section describing a test and evaluation plan for further R&D if the transition plan is evaluated as being successful. You must also submit your Phase II Cover Sheet & Company Commercialization Report electronically and mail a hard copy to the Navy STTR Program Office at the address above. While Phase I proposals with the option will adhere to the 25 page limit (section 3.3), Phase II proposals together with the Phase II option will be limited to 40 pages (unless otherwise directed by the TPOC or contract). The transition plan should be in a separate document.

The Navy will evaluate and select Phase I proposals using scientific review criteria based upon technical merit and other criteria as discussed in this solicitation document. Due to limited funding, the Navy reserves the right to limit awards under any topic and only proposals considered to be of superior quality will be funded. The names of firms whose proposals have been selected for further consideration will be posted by topic number on the Navy SBIR/STTR Website, under "What's New", "STTR Selections", within 3 months of the proposal deadline. In addition, the abstracts of companies that have received Phase I awards will be posted on the website within 5 months of proposal deadline.

Phase I awardees should submit a 5-page preliminary plan for Phase II to the Navy STTR Program Manager at the address above, 5 months and 2 weeks after contract award. However, only those Phase I awardees which have been invited to submit a formal Phase II proposal by the TPOC will be eligible for a Phase II award (with the exception of Fast Track Phase II proposals per section 4.5) . If you have been invited to submit a Phase II proposal to the Navy TPOC, get a copy of the Phase II proposal preparation and submittal guidelines from the Navy SBIR/STTR website.

ELECTRONIC SUBMISSION OF PROPOSAL COVER SHEET AND COMMERCIALIZATION REPORT:

Submit your DOD Proposal Cover Sheet (formerly Appendix A & B) and the DOD Commercialization Report (formerly Appendix E) to the Navy using the DOD online submission at http://www.dodsbir.net/sbirsubmission and as discussed in Section 3.4b and 3.4n of this solicitation. This site allows your company to come in any time (prior to the closing of the solicitation) to edit or print out your appendices. **The Navy WILL NOT accept any forms from past solicitation books or any electronic download version except those from the DOD SBIR Website as valid proposal submission forms.** Detailed instructions can be found by selecting the Help button on this site once you have registered. If you have any questions or problems with the electronic submission contact the DOD SBIR Helpdesk at 1-800-382-4634.

ELECTRONIC SUBMISSION OF PROJECT REPORTS:

The submission of an electronic Phase I Summary Report will now be required at the end of Phase I. This Summary Report is submitted in addition to the full Phase I final report hard copy that is mailed to the address above. The Phase I Summary Report is a non-proprietary summary of Phase I results and should include potential applications and benefits and not exceed 750 words. It should require minimal work from the contractor because most of this information is required in the final report. The summary of the final report will be submitted through the Navy SBIR/STTR Website at: http://www.onr.navy.mil/sbir, click on "Submission", then click on "Submit a Phase I or II Summary Report".

NAVY FAST TRACK DATES AND REQUIREMENTS:

All Fast Track Applications and required information must be sent to the Navy STTR Program Manager at the address listed above and to the designated Contracting Officers Technical Monitor (the Technical Point of Contact (TPOC) for the contract and the appropriate Point of Contact at the end of this Introduction). The following dates and information are required by the company to qualify for the FAST TRACK program. All of the requirements listed in the Fast Track Section of the front of this solicitation must be met. The information provided below provides specific dates and some additional information that is required by the Navy STTR Program Office.

Party/Days After Phase I Award	**Required Deliverables**
STTR Company / 150 Days	- Fast Track Application and all supporting information. (See instructions in the DOD section of this Solicitation) - Phase II 5 Page Summary Proposal, as required of all Phase I Projects as described in Navy STTR Website listed above. (It is strongly recommended that if you are contemplating the submittal of a Fast Track Application, you make your intention known to your technical point of contact and the STTR Program Manager) - Request to initiate Phase I option (interim funding) which must have been included in the original Phase I proposal
Navy / 181 Days	- Navy will initiate option funding if all requirements are met.
STTR Company /181 - 200 Days	- Phase II Proposal - Phase I Final Report
Navy / 201 - 215 Days	- Navy will formally Accept or Reject your Phase II proposal.
STTR Company /260 Days	- Proof that Funding has been received by STTR company.

PROPOSAL SUBMISSION CHECKLIST:

All of the following criteria must be met or your proposal will be REJECTED.

1. The Navy will not accept any proposals from companies that have not submitted the DOD Proposal Cover Sheet (formerly Appendix A & B) and the DOD Commercialization Report (formerly Appendix E) electronically over the Internet. After they are submitted electronically, these forms must be printed out directly from this site and be included with the entire proposal that is mailed to the Navy and received by 12 April 2000.

2. Your Phase I proposed cost for the base effort cannot exceed $70,000. Your Phase I Option proposed cost cannot exceed $30,000. The costs for the base and option should be clearly separate, and identified on the Proposal Cover Sheet, in the cost proposal, and in the work plan section of the proposal.

4. Your proposal must be received on or before the deadline date. The Navy will not accept late proposals or incomplete proposals. If you have any questions or problems with submission of your proposal, allow yourself time to contact the Navy or DoD SBIR Helpdesk and get an answer to your question. Submit electronic Internet forms early, as computer traffic increases, computer speed slows down. <u>Do not wait until the last minute.</u>

NAVY STTR 00 TOPIC DESCRIPTIONS

N00-T001 **TITLE: High-Gain Amplifier Technology for a High Data-Rate Digital Link**

TECHNOLOGY AREAS: Materials/Processes, Electronics

OBJECTIVE: Develop an amplifier technology for low-noise amplification of low-level, high-speed signals having pure sine wave (narrow band width), square wave (NRZ logic) and discrete pulse (RZ logic) shapes. This will enable improvements in a wide range of secure communications, radar, and surveillance functions in the military and improve signal quality possible from arrayed processors and low radiated power rf systems. Define a quantitative ranking scale for amplifier specifications that makes explicit how signal shape impacts the relative importance of phase and amplitude noise, peak gain and gain uniformity, dispersion, intermodulation, power consumption, and operating temperature. The goal is to define the best small signal amplifier technology for the three leading candidate technologies for high speed digital systems: superconducting JJ, InP HBT, and optoelectronics and each signal shape.

DESCRIPTION: In both optoelectronic and electronic receivers, low noise amplifiers are needed at the input to the electrical processor. Photodiodes have demonstrated bandwidths over 40 GHz while small circuits have internally clocked at 68 and 770 GHz in HBT and JJ. Superconducting digital electronics needs amplification of the signals before they are passed to room-temperature semiconductor based circuits due to their inherent RZ, 2 mV-ps pulse area. Today, this involves amplification of pulses with amplitudes of 200-300 uV to a few hundred mV clocked at 5-20 GHz, sometimes by conversion to NRZ waveforms. Purely digital free space signal transmission is increasingly attractive given the precedence of fiber optic communication. For this application, an amplifier capable of handling a 40-100 GHz square wave input signal with 5 ps rise/fall times, is needed as drivers of microwave power amplifiers. Both electrical and optical interfaces have been demonstrated for data rates up to a few Gbit/s without any WDM. The work should focus on higher data rates (10-20 Gbit/s) while minimizing power consumption and simplifying packaging. Approaches that demonstrate extendibility to data rates of 40-50 Gbit/s are preferred. This amplifier technology should not be application specific but may vary with pulse shape and initial amplitude. The amplification scheme may consist of one or more amplifier stages, including on-chip superconducting amplifiers and external semiconductor amplifiers, operating at different temperatures between 4 K and 400 K. Determination of amplification factors, noise figures, power consumption, and demonstrations that thermal modeling predicts the operating temperatures of different amplifier stages, is an important aspect of this research. Natural compatibility among technologies should be emphasized. Utilization of COTS components is preferred.

PHASE I: Evaluate the amplification requirements for a variety of applications with different signal shapes and input amplitudes. Design amplification schemes that are suitable for at least two of the applications listed. Experimentally verify at least one of these amplification schemes and characterize it in terms of gain, bandwidth, power consumption, and noise.

PHASE II: Build and demonstrate a multi-channel, low-noise amplifier technology suitable for high data rate digital links, and low amplitude electrical input signals. The demonstration must include integration with at least one of the applications for which the technology is deemed suitable.

PHASE III: Produce a self-contained prototype of a system containing the demonstrated amplifier technology for the chosen application.

COMMERCIAL POTENTIAL: This research will lead to the development of a range of multi-channel, low-noise, broadband, microwave amplifier products, including driver stages for power amplifiers, RF buffer amplifiers, low-noise receiver amplifiers. This amplifier technology will also enable the realization of the high-performance superconducting electronics technology, which has a number of promising applications in the scientific instrumentation and communications equipment. Markets including ADC/DAC components, transient digitizers, digital signal processors, true-time delay, correlators, fast memory and processors.

KEYWORDS: Broadband amplifier, optoelectronics, digital superconductivity, hybrid technology, cryogenic electronics, low noise amplifier

N00-T002 **TITLE: Wide Bandgap Semiconductor Limiters**

TECHNOLOGY AREAS: Sensors, Electronics, Battlespace

OBJECTIVE: This work seeks to exploit recent advances in wide bandgap semiconductor (WBS) materials to develop high power, high speed PIN microwave limiters.

DESCRIPTION: As a result of their high breakdown field (~ 3 MV/cm) and high carrier saturation velocity (~2.0x107 cm/s), the WBS (namely SiC and GaN) are ideal candidate materials for the realization of high power, high-speed microwave limiters and switches. SiC has the added advantage of a high thermal conductivity (up to 4.9 W/cm K, GaN has a thermal conductivity of ~2

W/cm K) while GaN has the benefit of heterostructures with AlGaN to tailor the band structure. These properties imply that SiC or GaN based PIN diodes can outperform conventional parts in insertion loss, power dissipation, and recovery time.

While PIN diodes have been studied in SiC and GaN for low frequency rectifiers and uv-detectors, little work have been done on their use as microwave devices [1]. Key issues include obtaining the required low background doping of the intrinsic region and realizing low resistance p-ohmic contacts. In addition, further understanding is needed of the fundamental (and defect assisted) breakdown in these materials to insure the realization of avalanche breakdown.

PHASE I: The contractor shall develop the process technology, device design, and device model for high power, high speed WBS microwave limiters for operation at 7-11 GHz. Design considerations shall include power dissipation level, recovery time, and insertion loss. It is highly desirable that a reliable, low specific contact resistance (<1x10-6 • -cm2) p-type contact be demonstrated to p+-material. A positive temperature coefficient of breakdown shall be achieved to support the existence of available breakdown in the device. Initial microwave power dissipation testing should be realized.

PHASE II: The contractor shall develop and demonstrate a WBG PIN limiter able to dissipate an average power of >50 W (> 2000 W peak, 10 microsecond pulse) of microwave power at 7-11 GHz with an insertion loss < 1.0 dB. A full characterization of diode insertion loss, survivability, and recovery shall be performed.

PHASE III: The contractor should be able to compete for the supply of high power, high speed limiters for microwave receivers such as for radar and electronic warfare.

COMMERCIAL POTENTIAL: This work is expected to engender faster, more robust, lower loss microwave limiters for microwave communications and satellite links.

REFERENCES: See for example: IEEE Transaction on Electron Devices, Special Issue on SiC Electronic Devices, vol 46, March 1999.

KEYWORDS: microwave: microwave limiters, wide bandgap, silicon carbide, gallium nitride

N00-T003 TITLE: <u>Wide Band Optoelectronic Field Effect Transistors</u>

TECHNOLOGY AREAS: Sensors, Electronics, Battlespace

OBJECTIVE: To develop solar blind GaN-based Optoelectronic Field Effect Transistors (OFETs) and Integrated Circuits for high-gain photodetectors.

DESCRIPTION: Visible-blind photodetectors are needed for the flame detection and for the detection of missiles and jet engines. The GaN-based OFETs will exhibit high-gain and are expected to be superior to two-terminal devices and suitable for integration with high-speed, high temperature wide-band gap semiconductor electronics.

PHASE I: Modeling and fabrication of prototype GaN-based Optoelectronic FETs and regular FETs. Assessment of technology and design of integrated circuits

PHASE II: Development of highly sensitive GaN-based OFETs and integrated circuits

PHASE III: Development of subsystems and systems for flame detection and for the detection of missiles and jet engines.

COMMERCIAL POTENTIAL: Flame detection is very important for power plants, gas turbine installations, and large-scale metal and semiconductor production facilities. These detectors will allow power industry to replace expensive and bulky systems by cheap and reliable GaN-based OFET detectors.

REFERENCES:
1. M. S. Shur and M. Asif Khan, GaN/AlGaN Heterostructure Devices: Photodetectors and Field Effect Transistors, MRS Bulletin, Vol. 22, No. 2, pp. 44-50, Feb. (1997)
2. M. S. Shur and M. Asif Khan, GaN and AlGaN Devices: Field Effect Transistors and Photodetectors, Gordon and Breach Science Publishers, Series Optoelectronic Properties of Semiconductors and Superlattices, Vol. 7 GaN and Related Materials II, pp. 47-86, S. Pearton, Editor (1999)

KEYWORDS: GaN, photodetector, visible-blind, Optoelectronic FET, missile detection, flame detection

N00-T004 **TITLE: High Dynamic Range Digital Waveform Synthesizer and Beam Forming**

TECHNOLOGY AREAS: Sensors, Electronics, Battlespace

OBJECTIVE: To exploit the digital transceiver array and beam forming accuracy by means of analog-to-digital and vice versa conversion for arbitrary wide-band waveform at tens G Hz RF.

DESCRIPTION: Digital Array Radar (DAR) uses fully digitized T/R modules in a novel antenna array architecture. Advanced techniques and recent developments, (e.g. direct digital sampling, high rate, high dynamic range A/D converters, high-speed digital computation and digital fiber-optic interfaces) are employed. These technologies, leveraged from the commercial telecommunications, computers, and networking markets, combine to provide several orders of magnitude improvement in Navy radar system performance and promise low risk/cost for near-term acquisitions. One of the main risk areas is the accuracy of digital transceiver of arbitrary waveform, bandwidth at tens G Hz & beyond.

PHASE I: Develop techniques for the design and analysis of all digital transceiver A/D converters and beam forming accuracy at tens G Hz frequency and high bandwidth waveforms.

PHASE II: Apply the results and techniques developed in Phase I to the design and analysis of prototype for digital array A/D & D/A beam forming test bed.

PHASE III Transition roadmap is confirmed as the Technology Innovation Transition in PMO 02 NAVSEA PEO Theater Air Defense and Surface Combatants. In case of L-band it will be used for Volume Search Radar for DD21. When the radiating front is in case of S-band, or C-band, DAR will be useful for AEGIS SPY-II upgrade, etc. digital military radar cheaper and more accurate at higher bandwidths and frequencies.

DUAL USE APPLICATIONS: Successful commercialization of this technology will impact digital telecommunication in the frequency band of digital cellular phones, digital TV, digital satellite linkage, being matured in return will make the digital weather radar more powerful to detect the low resolution tornado core in mid-west region.

REFERENCES:

1. S. Norsworthy, R. Schreier, G. Temes, “Delta-Sigma Data Converters,” IEEE Press , 1997
2. Digital Cellular Phones, e.g. Nokia and other name brand
3. Digital CD ROM,
4. Digital Car Antenna
5. Digital HD TV
6. Digital Satellite Transmission
7. Digital Video Transmission from UAV

KEYWORDS: Dynamic Range, Sigma-Delta ADC & DAC, Direct Digital Synthesizer, Digital Array Radar, Beam Forming

N00-T005 **TITLE: Embedded Wireless Communications Capability**

TECHNOLOGY AREAS: Information Systems

OBJECTIVE: Investigate technologies for communication badges.

DESCRIPTION: Today’s sailors use two types of wireless handsets to meet their communication needs--one handset for netted talk groups using a push-to-talk similar to walkie-talkies and another handset for dial telephone service similar to a cellular telephone. Although technology combining these services in one handset is becoming available, the Navy cannot afford to equip every sailor on a ship with these expensive handsets. The cost and inconvenience of battery management associated with these handsets remains an additional burden. Embedding wireless communications technology in low cost multifunction Smart Cards offer an attractive alternative to these traditional wireless handsets so that every sailor would be issued a communication badge. These communication badges could be designed to provide touch activation, voice activated dialing, geolocation, health status monitoring, submersible to 10 meters, and support external devices including headset, barcode reader, imaging devices and radiation monitors. Cost effective methods for producing communication badges needs to be investigated. Ultrawideband and conventional narrowband approaches are encouraged.

PHASE I: Investigate the scientific, technical, and commercial merit and feasibility of producing Smart Card communication badges.

PHASE II: Build, test, and optimize a prototype system using shipboard wireless communication badges.

PHASE III: Once a prototype communication badge system has been shown to meet Measures of Effectiveness and Measures of Performance the technology can be transitioned in one of several ways. It can be developed as a commercial product for use in industrial and business applications, it can be marketed as an aftermarket enhancement to the wireless provider’s system, or it can be incorporated as part of a larger shipboard program such as the aircraft carrier program office’s Integrated Communications and Advanced Networks (ICAN) effort or DoD Smart Card programs.

COMMERCIAL POTENTIAL: The private-sector application of low cost communication badges developed under this STTR is applicable to industrial and business applications.

REFERENCES:
1. ISO 7810: 1995, "Identification Cards – Physical Characteristics."
2. CAPT James Hoffman, "Wireless and the Navy", Presentation to the Federal Wireless Working Group, Charleston, SC, May 11, 1999.
3. W. Rankl & W. Effing, SMART Card Handbook, John Wiley & Sons, New York, 1997.
4. T. S. Rappaport, Wireless Communications: Principles and Practice, Prentice Hall PTR, Upper Saddle River, New Jersey, 1996.
5. H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech House, Boston MA, 1999.
6. Ultrawideband Working Group Web Page, http://www.uwb.org.

KEYWORDS: Smart Card, Shipboard, Wireless, Communications, Low Cost, ID Card

N00-T006 **TITLE: <u>Nitride Semiconductor Substrates</u>**

TECHNOLOGY AREAS: Sensors, Electronics, Battlespace

OBJECTIVE: The objective will be to identify and develop/transfer the most promising technology for the growth of large diameter nitride semiconductor boules for substrates for AMRFS power MMICs, Solar Blind UV sensing, and Blue lasers etc.

DESCRIPTION: Extremely high power solid state devices under investigation at present use SiC substrates because of the high thermal conductivity. However if GaN substrates could be made with large area, device technology would be far simpler, and more affordable, by avoiding hetero-junctions between GaN and sapphire, or SiC.

PHASE I: Candidate growth techniques will be critically examined and tested. The process most likely to succeed will be identified for phase II down select.

PHASE II: A prototype technology will be developed for pilot production and sample distribution or film growth.

PHASE III: Extremely high power wide band amplifiers on GaN substrates will be available for testing.

COMMERCIAL POTENTIAL: Blue laser development will be massively accelerated, and microwave/millimeter wave amplifiers will be very strong commercial items.

REFERENCES:
1. Abstracts from ONR workshop on Bulk Nitride Semiconductors to be held NRL Nov 23/24 (1999)
2. Proceeding of the Int. Conf. on Nitride Semiconductors – Montpellier France (1999)
3. Gallium Nitride and related Semiconductors. EMIS data reviews, INSPEC/IEE (1999) Ed. J.Edgar, et al.

KEYWORDS: Semiconductor, group 3 nitrides, substrates, boule growth

N00-T007 **TITLE: <u>On Chip Delivery of Cooling Power at Cryogenic Temperatures</u>**

TECHNOLOGY AREAS: Sensors, Electronics, Battlespace

OBJECTIVE: Development of high efficiency cooling systems with low parasitic noise for removal of heat from the surfaces of cryogenically cooled electronics and sensors.

DESCRIPTION: Cryogenic cooling has become a widely adopted technique to improve the performance of electronics and sensors. RF receiver front-ends and DDS, infrared (IR) imagers, and ultra-sensitive magnetic signature sensors are some of the devices that exhibit improved performance when cooled in their space, military, and commercial applications. Sensor sensitivity in general depends on reducing the background noise due to thermal fluctuations and stabilizing the device's temperature dependent calibration. The power consumed by digital devices can be lowered when signal amplitudes are reduced as is possible when the thermal noise is also reduced by operation at sub-room temperatures. Active localized cooling can be used to prevent thermal run-away in high-density processor chips. Processing speed is increased by decreased resistance. Some high performance technologies such as superconductivity are available only at cryogenic temperatures. Adoption of any performance enhancing application of cryogenics is enabled by a cooling system that is totally transparent to the user – fully self-enclosed, energy efficient, serviced infrequently or never, and delivering cooling exactly where it is needed. It also must be a small fraction of the system cost, which is possible only if most of the parts are standardized. Moreover, since temporal variations in temperature may result in a degraded signal, it is desirable to keep such fluctuations below 10-3 Kelvin at 77K. Heat pipes, thermoelectric coolers, high-conductivity flexible thermal links, and cryogenic refrigerants pumped through micro-pipes integrated into the substrate/MCM are some of the technologies of interest. Heat removal efficiency per unit electrical power expended; thermal fluctuations and hydrodynamic and electromagnetic noise at the device to be cooled; manufacturability, cost estimate, and prospects for ability to standardize cryocooler required for a wide variety of devices are the primary technical evaluation criteria to be used in evaluating proposals.

PHASE I: Demonstrate experimentally the technical feasibility of proposed cooling technique for simultaneously providing a 77K base temperature at each of 2 sensors (of nature agreed to by ONR) separated by a cm or more. Develop an implementation strategy showing feasibility of manufacturing; adaptability to a variety of configurations of devices needing cooling; analysis of issues to successful deployment on moving, vibrating, and rolling platforms; power requirements; maintenance, and cost.

PHASE II: Design, fabricate, and test of a technology demonstration unit (TDU) containing all the parts needed in a fielded system and cooling at least 2 separated devices. Demonstrate performance characteristics of the system under various operating conditions and environmental factors. Measure or develop calibrated method to quantitatively predict the effects of variable gravitational force or platform orientation in an unshielded environment and EMI and thermal fluctuation in the vicinity of the devices arising from the cooling system. Develop a commercialization-transition to Phase III plan, including description of strategy for developing a commercially viable technology.

PHASE III: Transfer the technology into a commercial application as well as an appropriate military application.

COMMERCIAL POTENTIAL: Cryocoolers are a critical enabling technology, especially for superconducting devices arrayed far apart. The phase II product would be sufficiently advanced to allow the technology's evaluation for integration into any application around 77K, including the cooling of high performance semiconductor chips, multi-channel wireless communications systems, and imaging SQUIDs used in medical research and non-destructive evaluation.

REFERENCES: T. Clem, "Superconducting magnetic sensors operating from a moving platform," IEEE Trans. Appl. Sup., vol. 5(2), p. 2124, 1995.

KEYWORDS: distributed cooling, electro-hydrodynamical cooling, thermoelectric cooling, cryocoolers, heat pipes, cryogenics

N00-T008 **TITLE: Uncooled Infrared Photon Detectors**

TECHNOLOGY AREAS: Sensors, Electronics, Battlespace

OBJECTIVE: Develop uncooled infrared photon detectors with high sensitivity and resolution in the mid and long wavelength range.

DESCRIPTION: Infrared photon detectors in the mid and long wavelength spectral region (3-12 • m) have applications in numerous defense, medical and industrial systems such as night vision, reconnaissance, guidance, ranging, thermal imaging, thermography, meteorological research and free-space communication systems. Currently, numerous approaches are being followed, including intrinsic detectors based on HgCdTe, InSb, InAsSb, InTlSb, InSbBi, and quantum well detectors based on GaAs/AlGaAs, InGaAsP/InP (QWIP) structures, type II InSb/InAsSb and InAs/GaInSb heterostructures. In most applications, this current technology makes use of cryogenic coolers which are ill-suited because of their short lifetime, added power consumption, weight, volume and cost. Uncooled detectors have generally been difficult to achieve due to fundamental problems such as fast Auger recombination and fast LO phonon scattering. Nevertheless, room temperature operation has been promisingly demonstrated for InAsSb, InSbBi, and type II InAs/GaInSb superlattice detectors in the 3-12 • m spectral range. The purpose of this effort is therefore to investigate and produce high sensitivity and high-resolution infrared detectors operating at room temperature in the 3-12 • m range.

PHASE I: Demonstrate the fundamental technologies necessary to produce high sensitivity and resolution infrared photon detectors operating at room temperature. Design and test optimum device structure.

PHASE II: Produce, package and demonstrate operational, high sensitivity and resolution infrared photon detectors.

PHASE III: Develop reliable infrared photodetector product operating at room temperature applicable for integration in night vision, reconnaissance, guidance, ranging, thermal imaging, thermography, communications, etc.

COMMERCIAL POTENTIAL: Potential defense-related applications for infrared photon detectors include enemy target detection, proximity fuze, smart bombs, LIDARs, active infrared countermeasure systems against missile threats, night vision in the battlefield, non-metallic land mine detection. These detectors will also be useful in medical applications such as thermal imaging for diagnosis of breast cancer, dental and thyroid diseases, non-invasive measurement of the oxygen level in organs during surgery, and blood sugar monitoring. Infrared detectors can also be used in industry in non-destructive testing and inspection techniques, for the fast detection of hidden cracks and non -uniformity, for the monitoring of chemical quality and process control, remote sensing and for free space communication.

REFERENCES: M. Razeghi, "Roadmap of semiconductor infrared lasers and detectors for the 21st century," in Photodetectors: Materials and Devices IV, ed. G.J. Brown and M. Razeghi, SPIE Proceedings Series, vol. 3629 (Bellingham, Wash.: SPIE-The International Society for Optical Engineering, 1999), 2-40.

KEY WORDS: IR detectors, uncooled detectors, sensors, countermeasure, night vision, thermal imaging